High Efficiency POL Module

MPX24AD05-TU

FEATURES:

- High Power Density Power Module
- 5A Maximum Load
- Input Voltage Range from 9.0V to 40.0V
- Output Voltage Range from 1.0V to 5.0V
- Excellent Thermal Performance
- 94% Peak Efficiency
- Enable Function
- Protections (OCP, SCP, OTP, Non-latching)
- Internal Soft Start with Pre-bias Output Start-Up
- Compact Size:15mm*15mm*7.4mm(Max.)
- Low Profile and Compact Size
- Pb-free Available (RoHS compliant)
- MSL 3, 245 ºC Reflow

APPLICATIONS:

- General Buck DC/DC Conversion
- Distributed Power Supply
- Server/Desktop Power Supplies

GENERAL DESCRIPTION:

The MPX24AD05-TU is a high frequency, high power density and complete DC/DC power module. The PWM controller, power MOSFETs and most of support components are integrated into one hybrid package.

The features of MPX24AD05-TU include voltage mode control with high phase margin compensation, internal soft-start, OCP and pre-biased output start-up capability. Besides, MPX24AD05-TU is an easy-to-use POL module, only input capacitors and output capacitors are needed to operate in all kinds of applications.

The compact size enables utilization of space for highly density point of load to save the space and area. The thermal pad can enhance heat transferring capability. It is suitable for automated assembly by standard surface mount equipment and is Pb-free and RoHS-compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

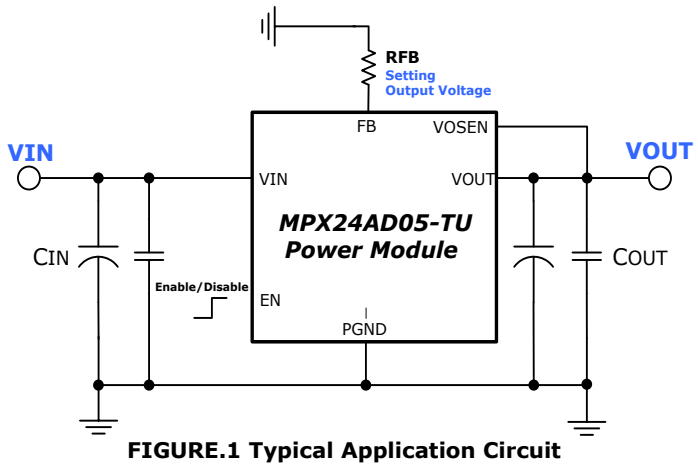


FIGURE.1 Typical Application Circuit

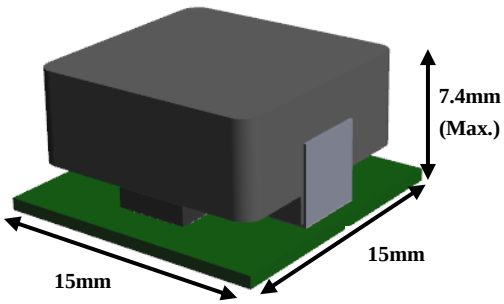
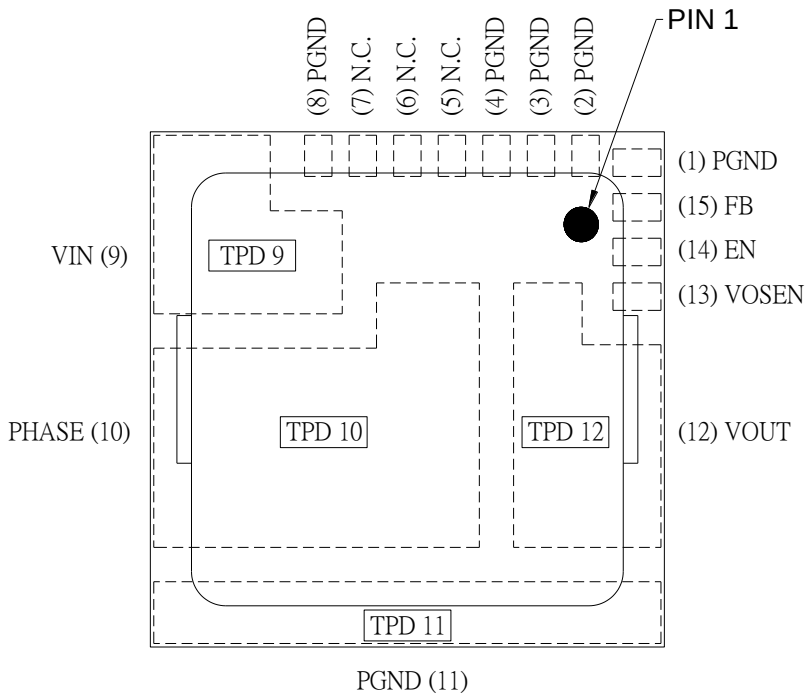


FIGURE.2 High Density Power Module

Vout	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
RFB (Ohm)	232k	140k	86.6k	63.4k	38.3k	26.7k	16.2k

PIN CONFIGURATION:

Top View



PIN DESCRIPTION:

Symbol	Pin No.	Description
PGND	1, 2, 3, 4, 8	Power ground pin for signal, input, and output return path. This pin needs to be connected to one or more ground plane directly.
N.C.	5,6,7	No connect
VIN (TPD 9)	9	Power input pin. It needs to be connected to input rail. It also needs to be connected to thermal dissipation layer by vias connection. Place the input ceramic type capacitor as closely as possible to this pin.
PHASE (TPD 10)	10	Phase node pin. Combined node of high-side MOSFETs, low-side MOSFETs, and output inductor. It needs to be connected to thermal dissipation layer by vias connection. If voltage spike stress and EMI are considered, a snubber circuit can be placed as near as possible to this pin so to absorb the spike and ringing.

PIN DESCRIPTION:(Cont.)

Symbol	Pin No.	Description
PGND (TPD 11)	11	Power ground pin and needs to be connected to PGND pins (1, 2, 3, 4, and 8), all are to be connected to one or more ground plane directly. This pin needs to be connected to thermal dissipation layer by vias connection. Place both the input and output ceramic type capacitors as closely as possible to this pin. If voltage spike stress and EMI are considered, the snubber circuit can be placed as near as possible to this pin so to absorb the spike and ringing.
VOUT (TPD 12)	12	Power output pin. It needs to be connected to output rail. It also needs to be connected to thermal dissipation layer by vias connection. Place the output ceramic type capacitor as closely as possible to this pin.
VOSEN	13	Output voltage sensing pin. Connect to output loading to eliminate the positive voltage loss along the trace and keep the regulation at loading. CAUTION: Do not leave this pin open.
EN	14	High level or floating enable depends on part number.
FB	15	Feedback input. Connect a resistor between this pin and ground for adjusting output voltage. Place this resistor as closely as possible to this pin and ground.

Part Number Define:

Part Number	Enable	Disable
MPF24AD05-TU	Floating	V_{EN}<0.4 V
MPN24AD05-TU	3.1 V <V_{EN}< 5.5 V	V_{EN}<0.4 V

ELECTRICAL SPECIFICATIONS:

Conditions: Ta = 25 ºC,unless otherwise specified.
Vin=24V, Vout=5.0V, Cin=100uF/50V(Aluminum Electrolytic Capacitors), 1uF/50V Ceramic X7R
Cout=330uF/POS-CAP×1, 100uF/Ceramic×3

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{Q(VIN)}$	Input supply bias current	Iout=0A Vin=24V, Vout=5.0V	-	34	-	mA
$I_{S(VIN)}$	Input supply current	Iout=5A Vin=24V, Vout=5.0V	-	1.12	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range		0	-	5	A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin=9V to 40V Vout=5.0V, Iout=0A Vout = 5.0V, Iout = 5A	-	0.1	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0A to 5A Vin = 24V, Vout = 5.0V	-	0.5	-	%
$V_{OUT(AC)}$	Output ripple voltage	Iout = 5A Vin = 24V, Vout = 5.0V	-	35	-	mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Positive step change in output current	0% to 50% to 0% of Full Load			5	%Vo
ΔV_{OUT-DN}	Negative step change in output current	0% to 50% to 0% of Full Load			5	%Vo
■ Other						
F_{OSC}	Oscillator frequency			300		kHz
$T_{(start)}$	Soft Start Time			3		mSec
OCP	Protection Output Current			9.5		A
V_{REF}	Referance voltage	$-40^0C \leqq Ta \leqq 85^0C$	0.693	0.7	0.715	V
R_{FB-TI}	Internal resistor between VOUT and FB pins		99	100	101	kΩ
■ Thermal Information						
Tc			-		+110	˚C
Ta	Ambient Temperature		-40		85	˚C
Rth(j_{choke}-a)	Thermal resistance from junction to ambient. (Note 1)			12		°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 80mm×80mm×1.6mm with 4 layers. The test condition is complied with JEDEC EIJ/JESD 51 Standards

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: Ta = 25 ºC,unless otherwise specified.
Cin=100uF/50V(Aluminum Electrolytic Capacitors), 1uF/50V Ceramic X7R
Cout=330uF/POS-CAP×1, 100uF/Ceramic×3
Test Board Information: 80mm×80mm×1.6mm, 4 layers, 1oz.

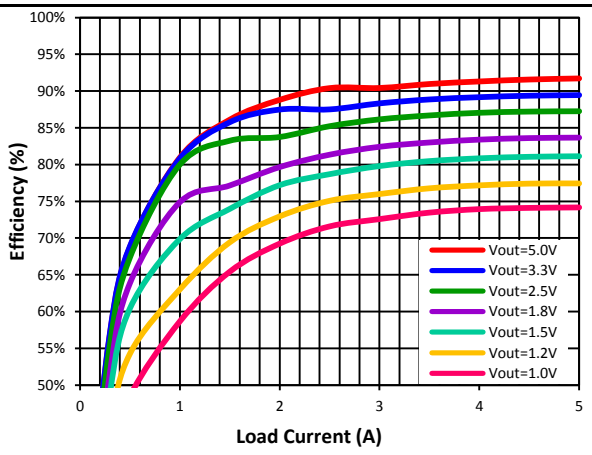


FIG.3 40Vin Efficiency V.S. Load Current

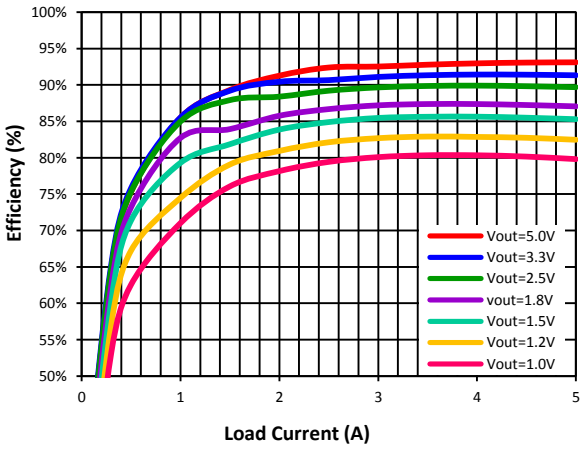


FIG.4 24Vin Efficiency V.S. Load Current

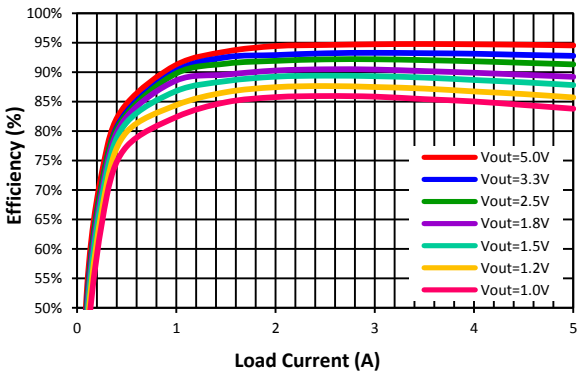


FIG.5 12Vin Efficiency V.S. Load Current

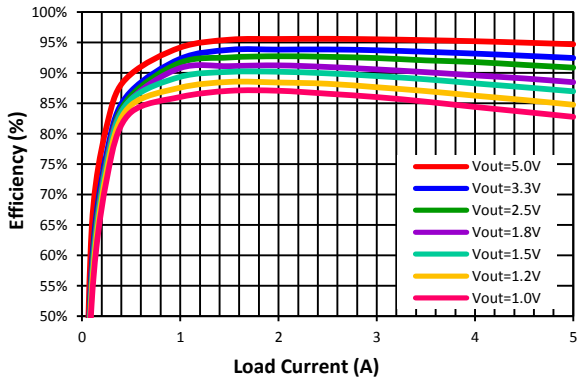


FIG.6 9Vin Efficiency V.S. Load Current

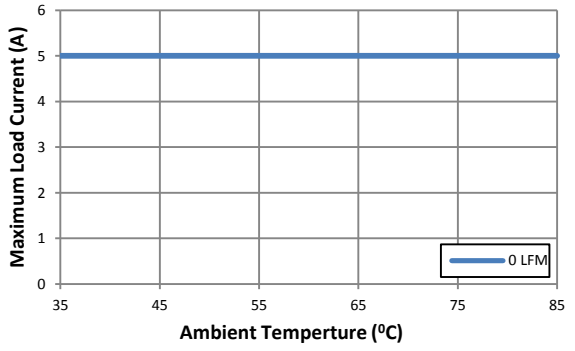


FIG.7 24Vin/5.0Vout Thermal De-Rating Curves

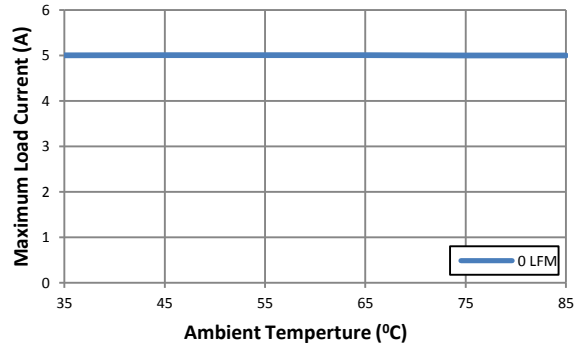


FIG.8 40Vin/5.0Vout Thermal De-Rating Curves

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: Ta = 25 ºC,unless otherwise specified.
Vin=24V,Cin=100uF/50V(Aluminum Electrolytic Capacitors), 1uF/50V Ceramic X7R
Cout=330uF/POS-CAP×1, 100uF/Ceramic×3
Test Board Information: 80mm×80mm×1.6mm, 4 layers, 1oz.

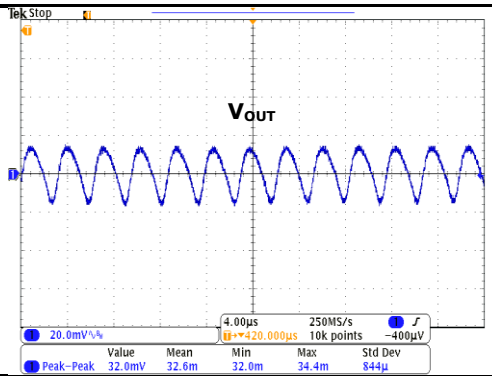


FIG.9 5.0Vout Output Ripple, at 5A Load Current

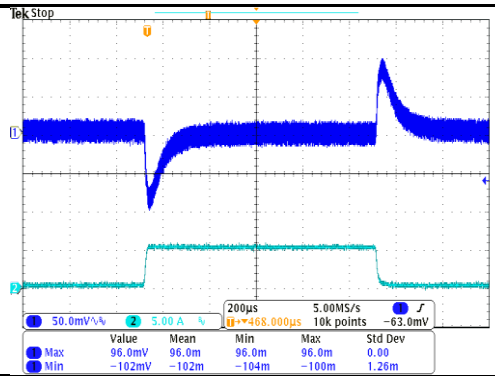


FIG.10 5.0Vout Transient Response, at 0A to 5A Load Current

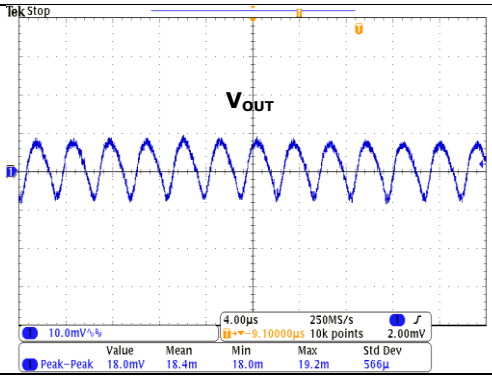


FIG.11 3.3Vout Output Ripple, at 5A Load Current

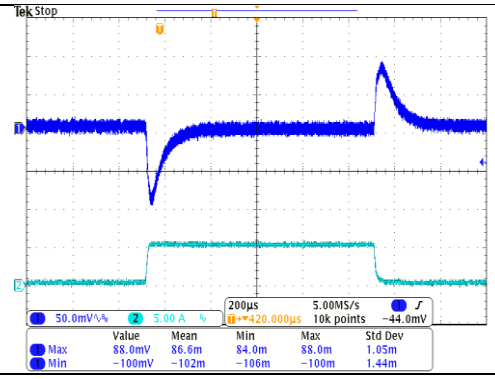


FIG.12 3.3Vout Transient Response, at 0A to 5A Load Current

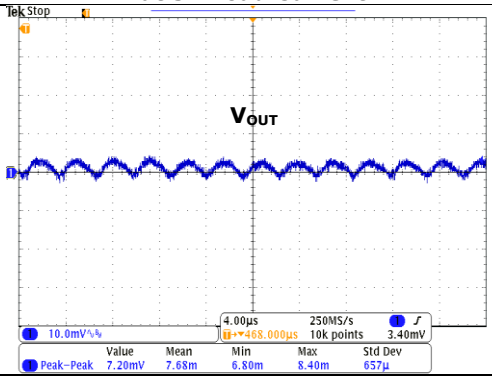


FIG.13 1.0Vout Output Ripple, at 5A Load Current

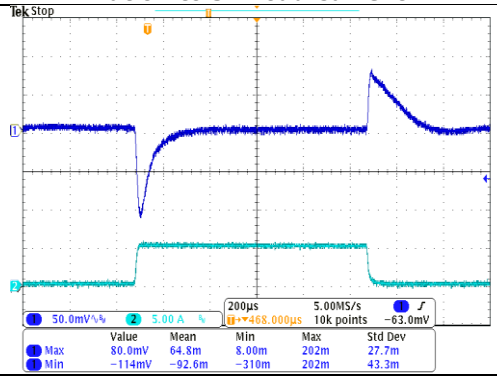


FIG.14 1.0Vout Transient Response, at 0A to 5A Load Current

TYPICAL PERFORMANCE CHARACTERISTICS:

Conditions: Ta = 25 ºC,unless otherwise specified.
Vin=24V,Cin=100uF/50V(Aluminum Electrolytic Capacitors) , 1uF/50V Ceramic X7R
Cout=330uF/POS-CAP×1, 100uF/Ceramic×3
Test Board Information: 80mm×80mm×1.6mm, 4 layers, 1oz.

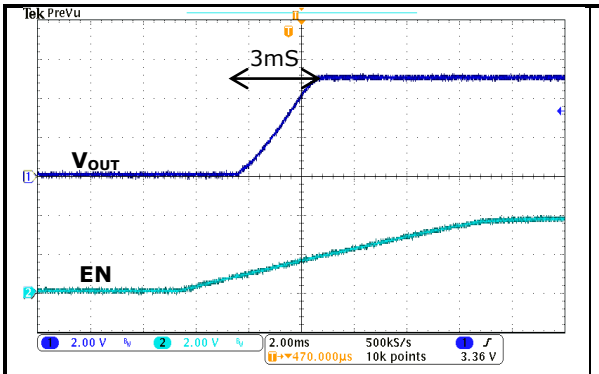


FIG.15 Enable Start-Up with Full Load

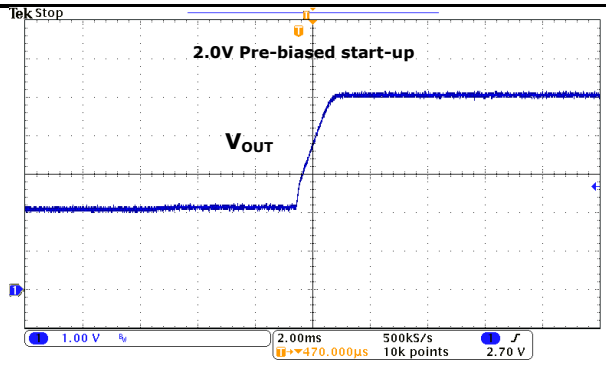


FIG.16 Start-Up with Pre-Bias Voltage

APPLICATIONS INFORMATION:

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is a possibility of sustained input voltage reversal which is not current-limited. For greatest safety, we recommend a fast blow fuse installed in the input supply line. The installer must observe all relevant safety standards and regulations.

For safety agency approvals, install the converter in compliance with the end-user safety standard.

PROGRAMMING OUTPUT VOLTAGE:

The MPX24AD05-TU has an internal 0.7V reference voltage. It only programs the dividing resistance R_{FB} which respects to FB pin and PGND. The output voltage can be calculated as shown in Equation 1.

$$VOUT = 0.7 \times \left(1 + \frac{100k}{R_{FB}}\right) \quad \text{(EQ.1)}$$

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 17.

1. The ground connection between pin 11 and pin 1 to 4 and 8 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place high frequency ceramic capacitors between pin 9 (VIN) and pin 11 (PGND) as close to module as possible to minimize high frequency noise.
3. Keep R_{FB} connection trace to the module pin 15 (FB) short.
4. The VOSEN pin can have remote trace layout to the local point sensing for output. It can eliminate the positive voltage droop on the trace to keep local regulation well.CAUTION: Do not leave VOSEN pin open.
5. Use large copper area for power path (VIN, VOUT, and PGND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
6. Avoid layout any sensitive signal traces near the pin 10 (PHASE).

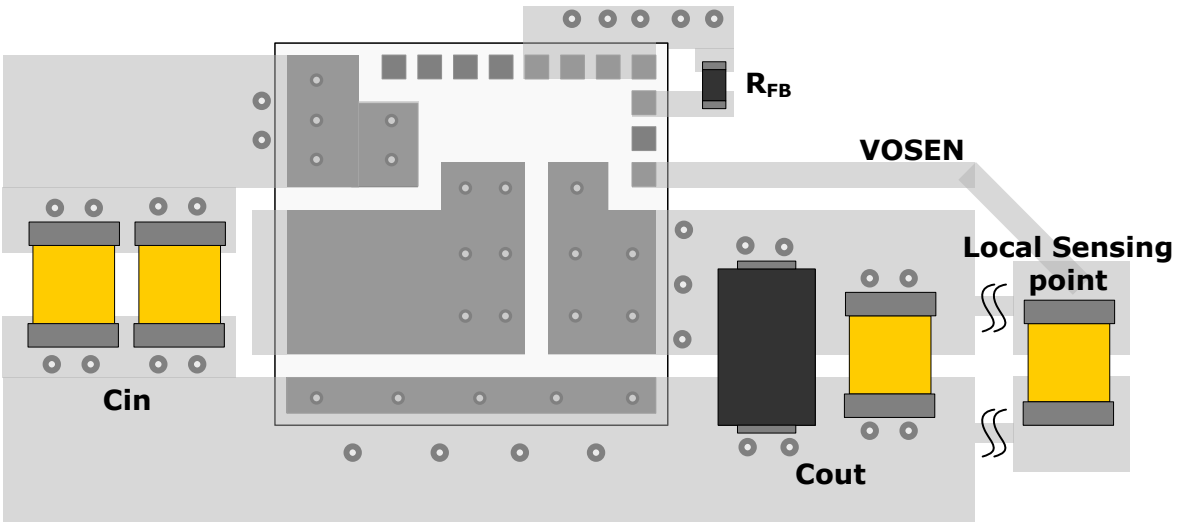


FIG.17 Recommendation Layout

Thermal Considerations:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 80mm×80mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 18. Then $Rth(j_{choke}\text{-}a)$ is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The output current ability is function of input/ output voltage and ambient temperature factor etc. The MPX24AD05-TU module is designed for using when the case temperature is below 110°C.

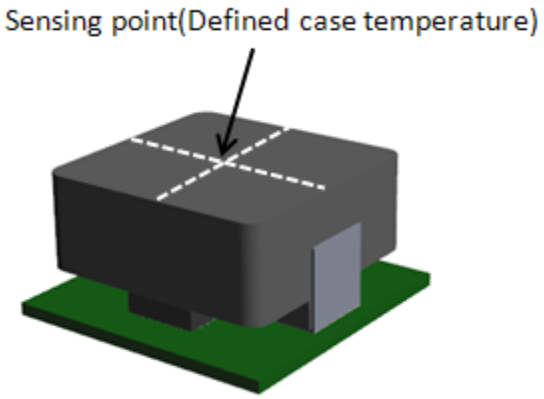


Figure 18. Case Temperature Sensing Point

REFLOW PARAMETERS:

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 19 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

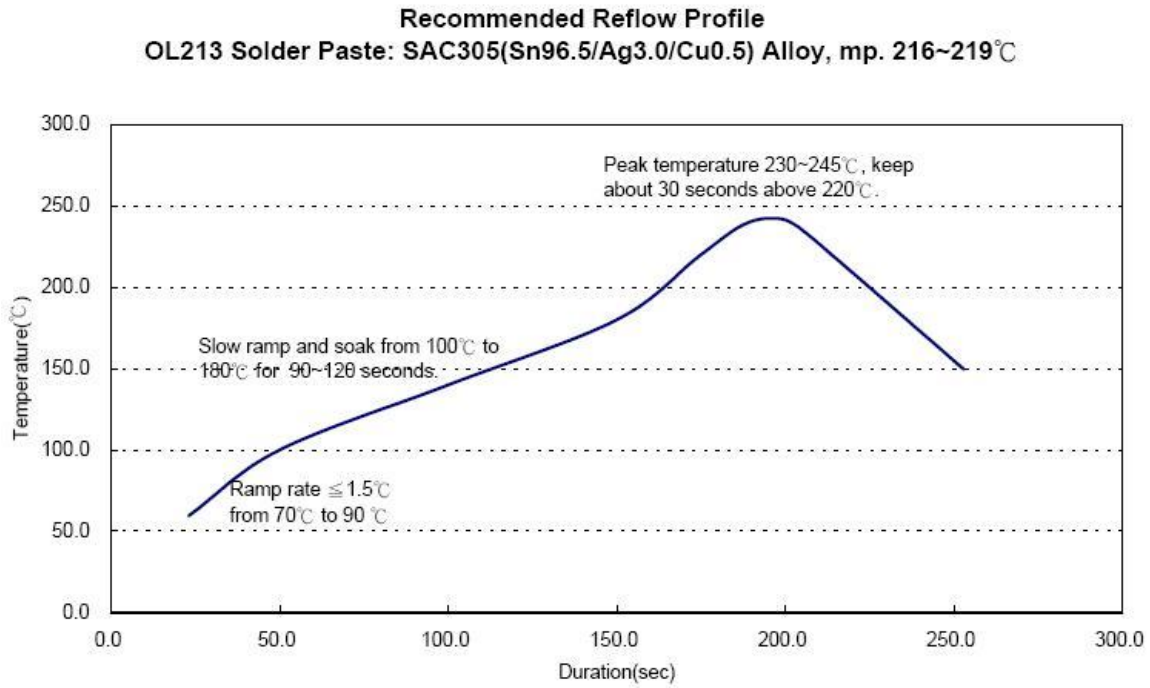
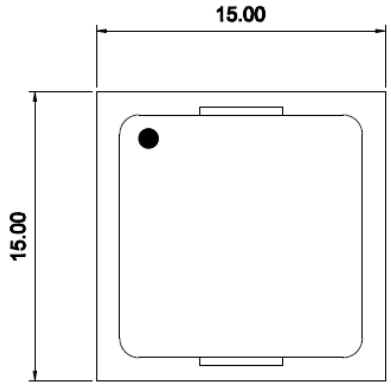


FIG.19 Recommendation Reflow Profile

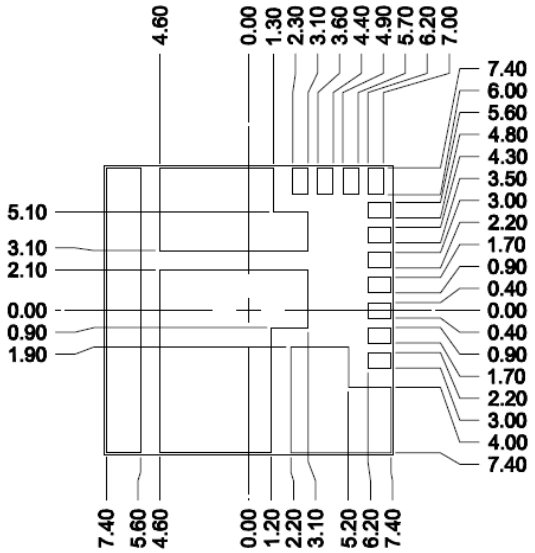
PACKAGE OUTLINE DRAWING:

Unit: mm

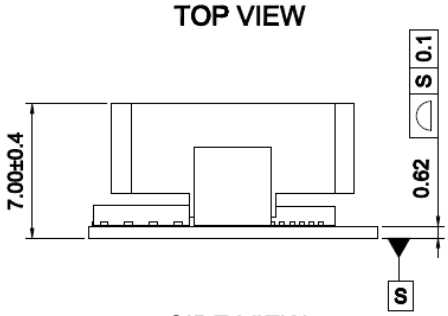
General Tolerances:±0.2mm



TOP VIEW



BOTTOM VIEW

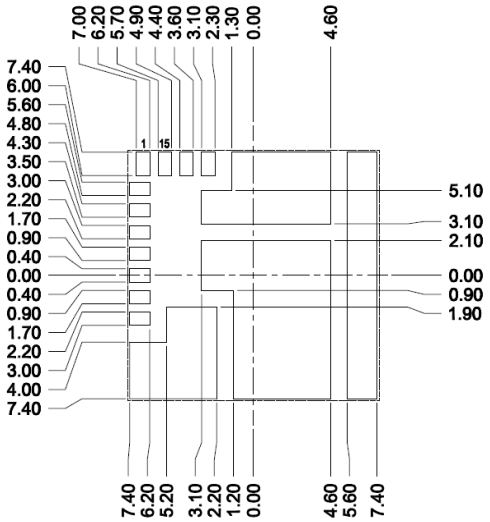


SIDE VIEW

LAND PATTERN REFERENCE:

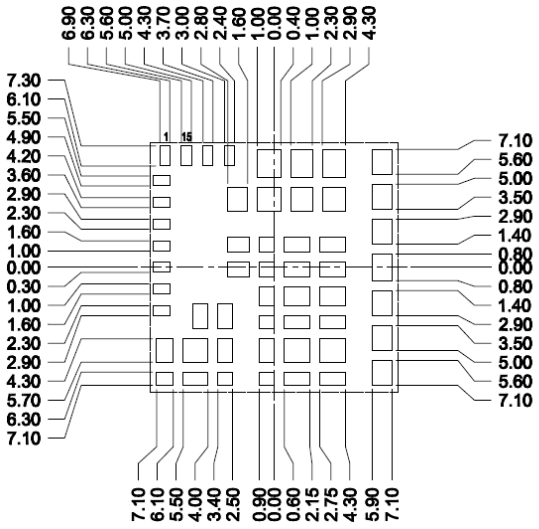
Unit: mm

General Tolerances:±0.2mm

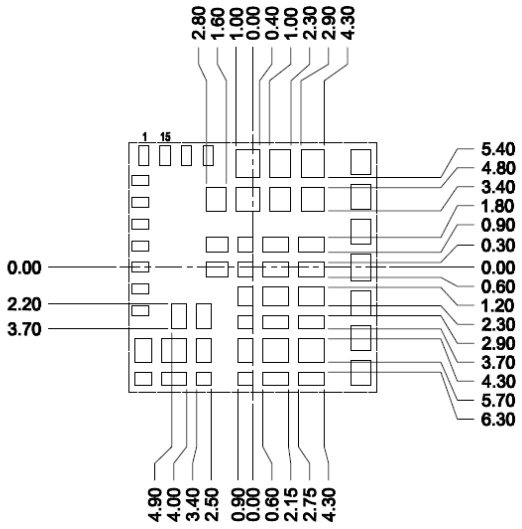


TOP VIEW

TYPICAL RECOMMENDED LAND PATTERN



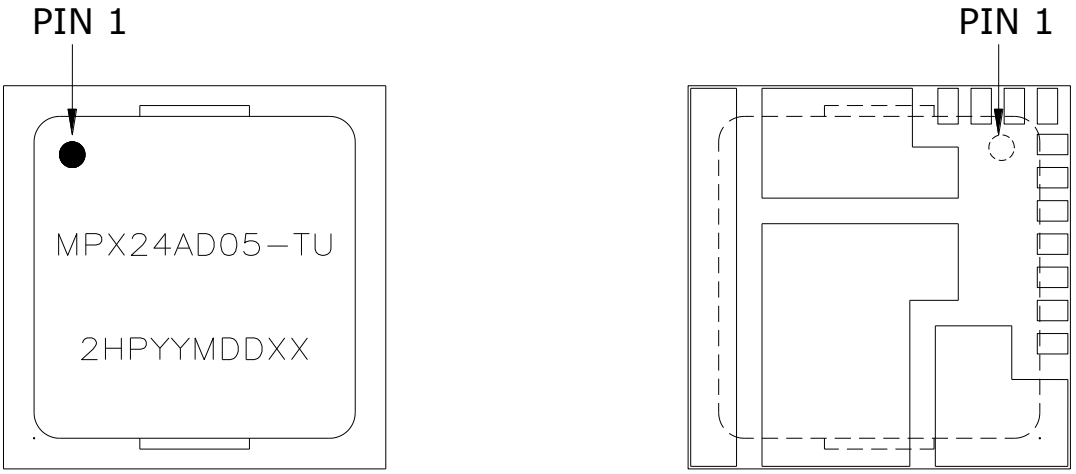
TOP VIEW – 1



TOP VIEW - 2

STENCIL PATTERN WITH SQUIRE PADS (STENCIL t=120μm)

MARKING DRAWING:



TOP VIEW

BOTTOM VIEW

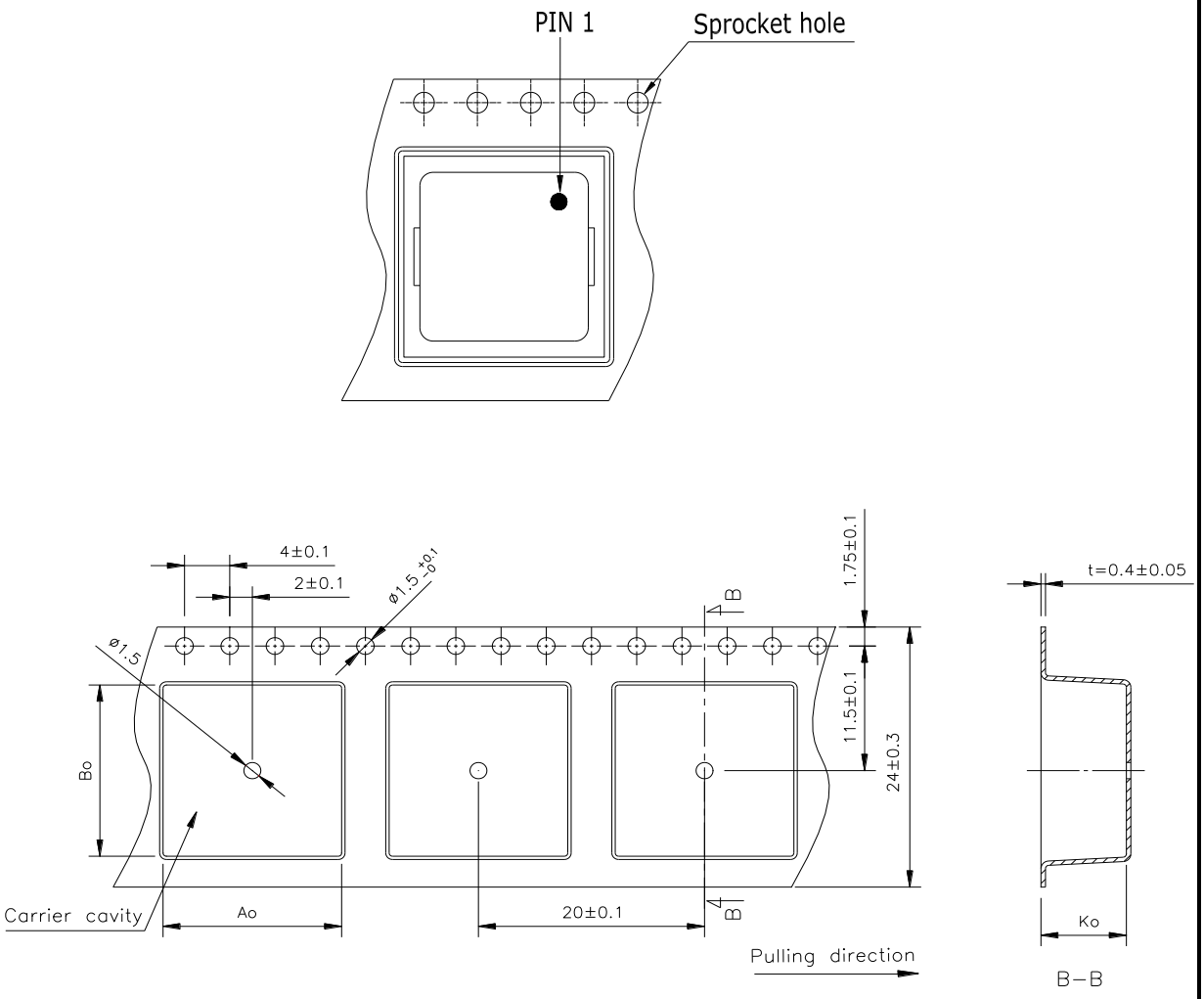
Marking note:

1. Circle represents the position of PIN1
2. MPX24AD05-TU represents the Product Name
   X : Reference Part Number Define
3. 2HPYYMDDXX represents the Lot Number

PACKING INFORMATION:

Unit: mm

Package In Tape Loading Orientation



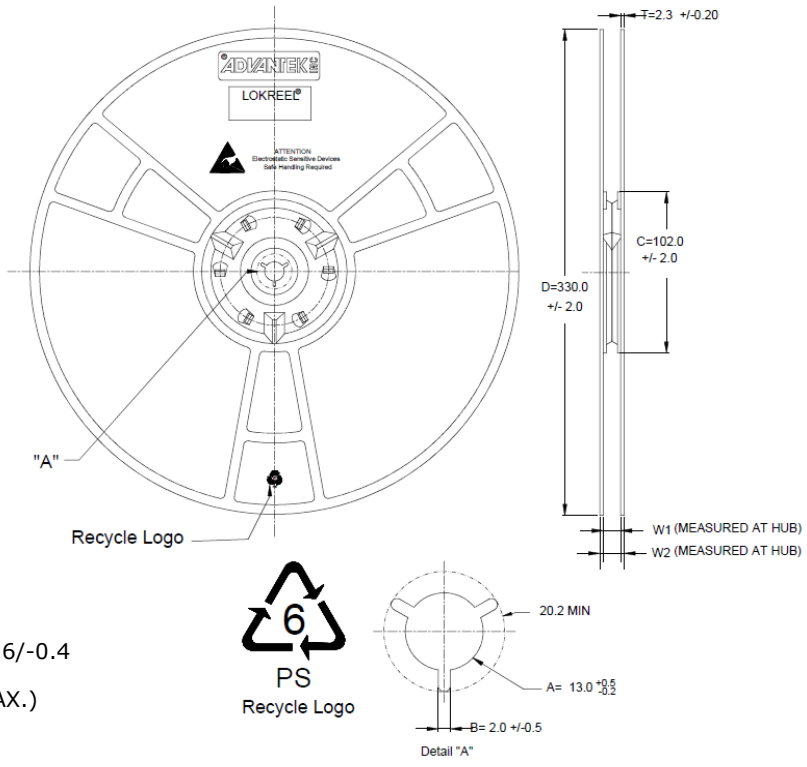
Carrier Tape Dimension

A0	15.8 ± 0.10
B0	15.8 ± 0.10
K0	7.55 ± 0.10

PACKING INFORMATION: (Cont.)

Unit: mm

Reel Dimension



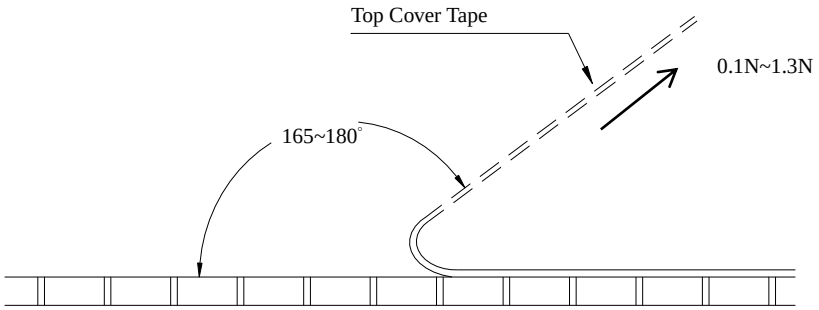
W1=24.8 +0.6/-0.4

W2=30.2 (MAX.)

Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall between 0.1N to 1.3N



REVERSION HISTORY:

Date	Revision	Changes
2014.10.02	00	Release the preliminary specification.
2014.10.06	01	Add thermal De-rating Curves
2014.10.14	02	1. Add Reflow Profile 2. Parted 2 part numbers depend on En control method
2014.11.11	03	Add Marking drawing and packing.
2014.12.05	04	1. PIN CONFIGURATION ● Add PIN 1 2. Modify MARKING DRAWING ● MPN24AD05-TU -> MPX24AD05-TU X：Reference Part Number Define ● Port Number -> Product Name 3. PACKING INFORMATION ● PIN 1 ，Top right corner -> Top left corner
2014.12.17	05	PACKAGE OUTLINE DRAWING ● END VIEW Hmax. 7.4 -> 7±0.4
2015.01.06	06	1. Modify MARKING DRAWING ● Modify DRAWING ● Blue circle representation position of PIN1 -> Circle representing position of PIN1 2. PACKING INFORMATION ● Pulling direction -> Pulling direction
2015.02.26	07	1. Thermal Considerations: ● Add Thermal Considerations ● Add Case Temperature Sensing Point 2. PACKAGE OUTLINE DRAWING ● Tolerances:±0.2mm -> General Tolerances:±0.2mm ● Modify Drawing , 15±0.1 * 15±0.1 → 15.00 * 15.00 3. Modify land pattern reference ● Tolerances to the second decimal place. 4. PACKING INFORMATION

		● PIN 1 ，Top left corner -> Top right corner